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Cadence, Imec Disclose 3-nm Effort

Cadence Design Systems and the Imec research institute disclosed that they are working toward a 3-nm tapeout of an unnamed 64-bit processor. The effort aims to produce a working chip later this year using a combination of extreme ultraviolet (EUV) and immersion lithography.

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Intel described 0.0312-mm2 high density and 0.0367-mm2 low-voltage SRAM bitcells made in its 10-nm process. Samsung's 6T 256-Mbit device has a 0.026-mm2 bitcell.

The Intel design shows 0.62–0.58x scaling compared to its 14-nm SRAM, maintaining Moore's law and "within 15 percent of the smallest reported 7-nm cell," said Intel's Zheng Gui, pointing to smaller 7-nm SRAMs from Samsung this year and TSMC at ISSCC 2017.

Intel Movidus TAKES AI TO Mobile Pcs

PARIS — It might not be too long before your average mobile PC will feature — on its motherboard — not just CPUs and GPUs but also an embedded AI inference chip, like the Intel/Movidius Vision Processor Unit (VPU).

The first clue for this scenario unfolded in Microsoft Corp.'s launch announcement today, at its Windows Developer Day, of Windows ML, an open-standard framework for machine-learning tasks in the Windows OS. Microsoft said that it is extending Windows OS native support for the Intel/Movidius VPU. Implied in the message is that Intel/Movidius has taken a step closer to finding a home not just in embedded applications, such as drones and surveillance cameras, but also in Windows-based laptops and tablets.

In a telephone interview with EE Times, Gary Brown, director of marketing at Movidius/Intel, confirmed, "Although today's announcement isn't about that [VPU integration on a mobile PC], yes, you will see VPU migrating into a PC motherboard."

Broadcom Equips Jericho2 With HBM2 And 2.5D

SAN JOSE, Calif. — Broadcom's latest communications processor rides a 2.5D chip stack with HBM2 memory. Jericho2 uses the boost in memory bandwidth to leapfrog the performance of OEM ASICs in high-end switches and routers.

The chip expands into networking the packaging technology pioneered by AMD, Nvidia, and Xilinx in high-end FPGAs and graphics processors. With its StrataDNX Jericho2, Broadcom also takes a small step toward open-programming environments by providing C++ tools for the chip to select customers.

The 16-nm processor, announced Tuesday (March 6), packs a whopping 208 50-Gbits/s PAM4 SerDes to deliver 10 Tbits/s of aggregate throughput, supporting up to 36 400-Gbits/s Ethernet links. It leads a wave of high-end networking devices aiming to enable 400-Gbits/s links in telcom core networks and large data centers.

Cypress Sees A Future For FRAM

TORONTO — Does ever-emerging Ferroelectric Random Access Memory(FRAM) have a role in autonomous vehicles? Cypress Semiconductor thinks so.

At the Embedded World trade show in Germany this week, the company unveiled a new serial nonvolatile memory family to meet the performance and reliability demands of mission-critical data capture. In an advance telephone briefing with EE Times, Sonal Chandrasekharan, senior director of Cypress' RAM Business Unit, said that the Excelon (FRAM) line was designed specifically for the high-speed nonvolatile data logging needed for autonomous vehicles. More broadly, the new FRAM line has applications in a broad range of advanced automotive and industrial applications.

Cadence, Imec Disclose 3-nm Effort

SAN JOSE, Calif. — Cadence Design Systems and the Imec research institute disclosed that they are working toward a 3-nm tapeout of an unnamed 64-bit processor. The effort aims to produce a working chip later this year using a combination of extreme ultraviolet (EUV) and immersion lithography.

So far, Cadence and Imec have created and validated GDS files using a modified Cadence tool flow. It is based on a metal stack using a 21-nm routing pitch and a 42-nm contacted poly pitch created with data from a metal layer made in an earlier experiment.

Imec is starting work on the masks and lithography, initially aiming to use double-patterning EUV and self-aligned quadruple patterning (SAQP) immersion processes. Over time, Imec hopes to optimize the process to use a single pass in the EUV scanner. Ultimately, fabs may migrate to a planned high-numerical-aperture version of today's EUV systems to make 3-nm chips.